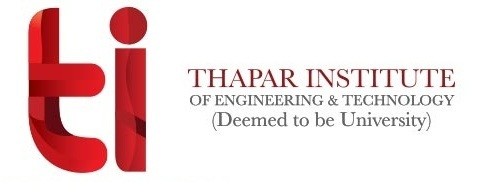
**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**



Analog IC Design

**Experiment-5**

**Submitted by**

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**M.Tech (VLSI Design)**

**Experiment-5**

**Aim**:

To implement a common source amplifier using diode connected load of gain 5 and analyse its transient and ac characteristics.

**Tool Used:**

LTspice

**Theory:**

When the input signal is applied at the gate terminal and source terminal, then the output voltage is amplified and obtained across the resistor at the load in the drain terminal. This is called a common source amplifier.

Common source amplifier is similar to the common-emitter follower of Bipolar Junction transistor. If we use P-channel FET, the polarity of the input voltage will be reversed.

For a Level 3 NMOS let’s assume

VDD = 1.8V

VT = 0.4V

VGS = 0.6V

Kn = 120µA/V2,

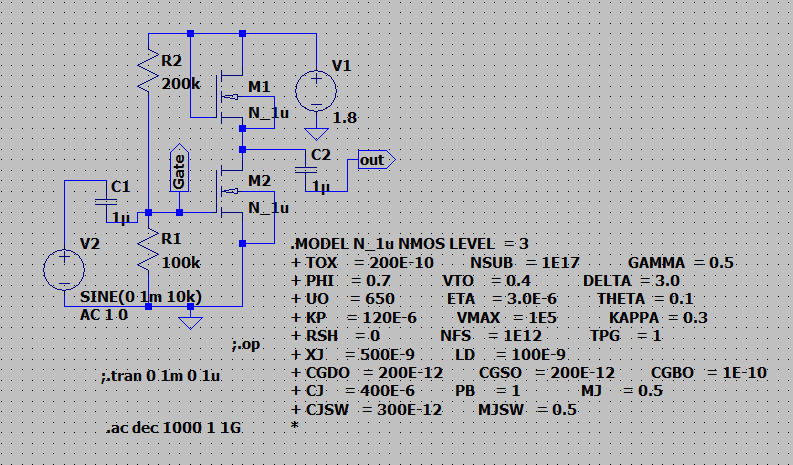
Which gives a value of (W/L) = (25) for 1mA ID.

Also, for these values’ gm is attained as 10mΩ-1, therefore for gain 10, RD is taken as 1KΩ.

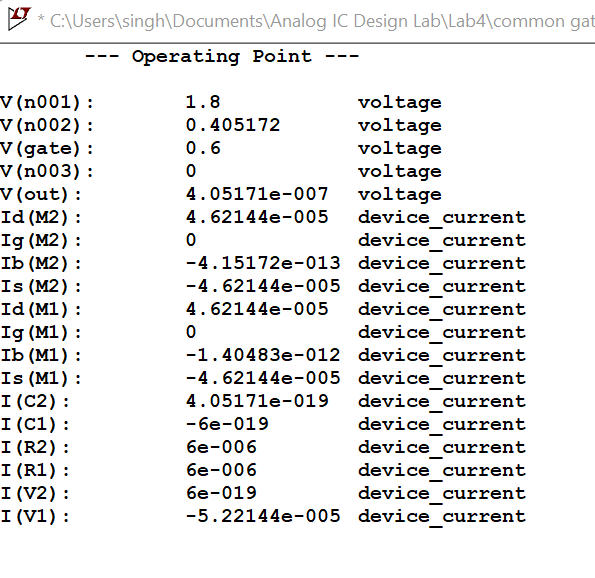
The value of VDS should be maintained above (VGS - VT = 0.6 - 0.4 = 0.2V) for the transistor to stay in saturation region.

As for M2, the width is taken as 250µm and the length is taken as 10µm and for M1, the width is taken as 50 µm and the length is taken as 50 µm.

**Circuit Schematic: [ Level 3 ]**

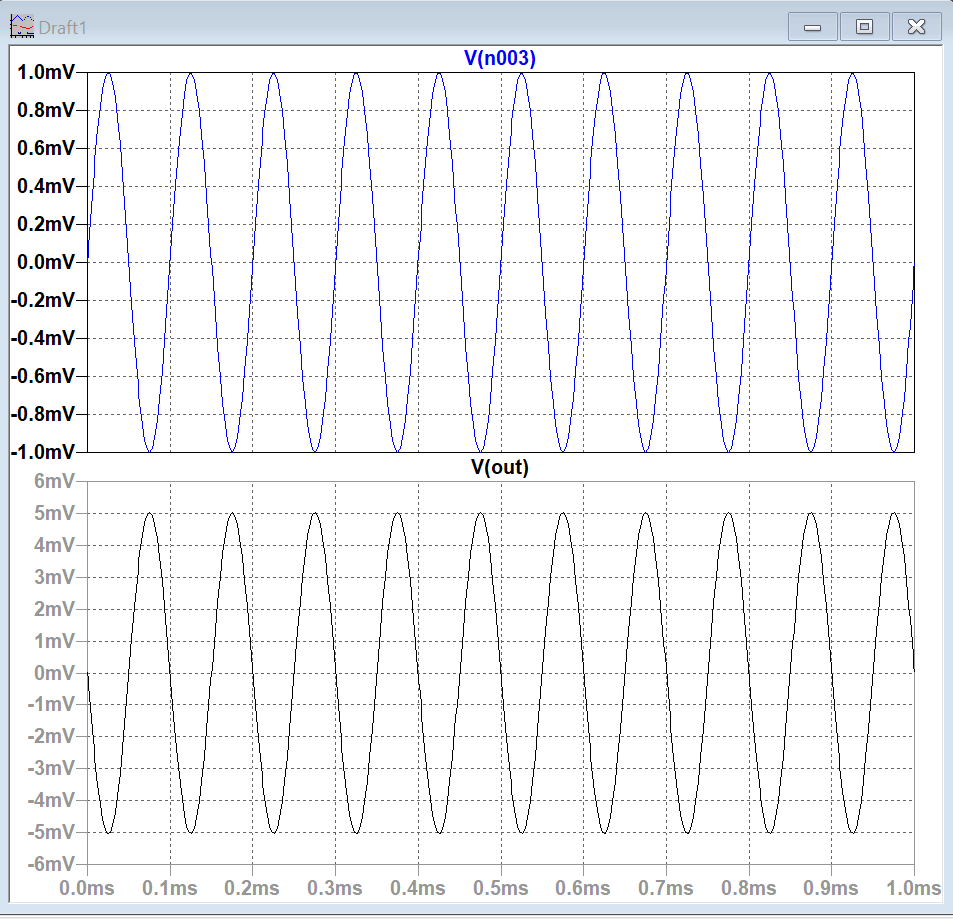
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**DC Operating Point**

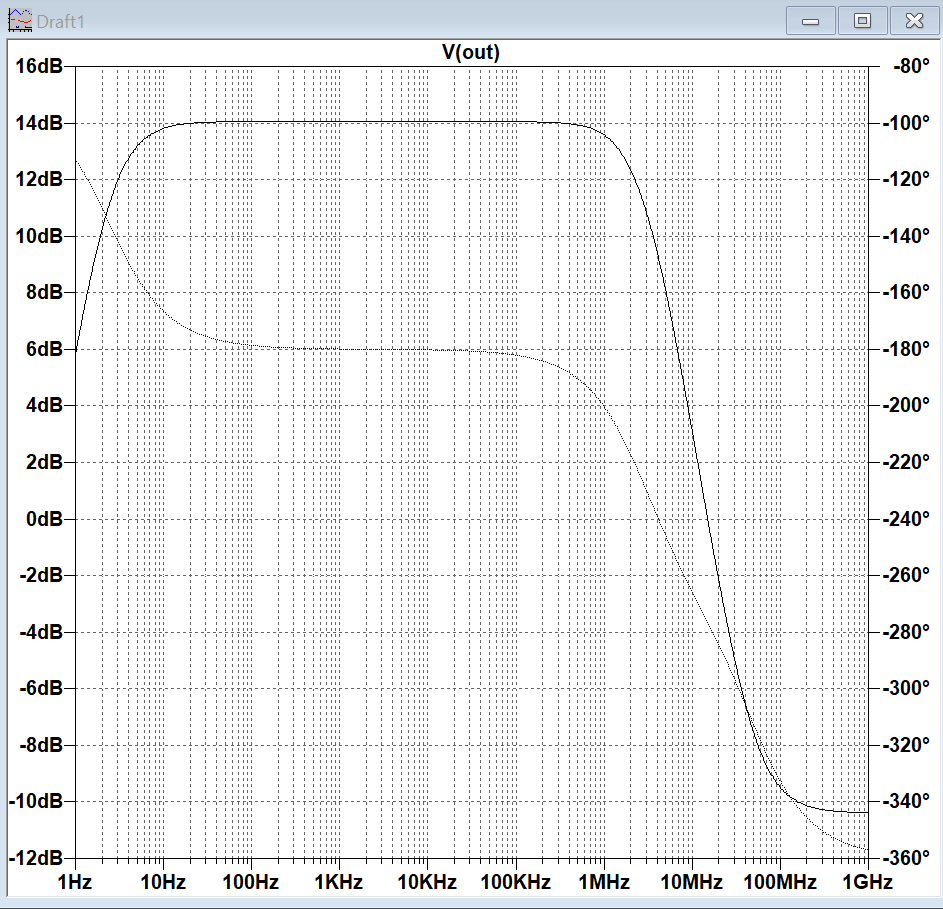
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**Output Waveforms:**

Transient Response:



AC Analysis:



**Result:**

The circuit is designed for a gain of 5 and the output is verified to be correct.

* Bandwidth is obtained to be: 3.17MHz
* Cutoff Freq: 3.17MHz, 2.36Hz